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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,286	02/12/2004	Makoto Onozawa	122.1581	3508

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EXAMINER	
AL NAZER, LEITH A	

ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,286	ONOZAWA ET AL.	
	Examiner	Art Unit	
	Leith A. Al-Nazer	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12 February 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,502,412 to Choi et al.

With respect to claims 1 and 12-14, Choi teaches a pre-drive circuit (figure 3) comprising: a plurality of drive systems each having an input amplifier circuit (50) for

amplifying an input voltage input to an input voltage terminal; a high level shift circuit (68 and 70) for shifting a level of a signal output form the input amplifier circuit; and an output amplifier circuit (72 and 76) for amplifying a shift signal output from the high level shift circuit, wherein each drive system has the same constitution (figure 3).

With respect to claim 2, Choi teaches a power supply terminal for supplying the drive power supply of the input amplifier circuit of the plurality of drive systems and a power supply terminal for supplying the drive power supply of the output amplifier circuit of the plurality of drive systems are provided separately (VDD, VB, and VCC in figure 3).

With respect to claims 3 and 4, Choi teaches waveform processing circuits (50A-50C) each of which is provided between the input voltage terminal and the input amplifier circuit of each of the drive systems.

With respect to claim 5, Choi teaches a constant voltage circuit (VDD) that generates a supply voltage for the waveform processing circuit by converting a voltage to be supplied to the power supply terminal for the input amplifier circuit and supplies the generated voltage as a supply voltage to the waveform processing circuit.

With respect to claim 6, Choi teaches each drive system including a low level shift circuit for shifting a level of a signal output from the input amplifier circuit to a signal referred to a negative reference voltage, and the high level shift circuit shifts the level of the signal output from the low level shift circuit (column 1, line 51 – column 2, line 9).

With respect to claims 7 and 11, Choi teaches each drive system including a waveform processing circuit (50A-50C) for processing a waveform of the signal output from the low level shift circuit, the high level shift circuit (column 1, line 51 – column 2,

line 9) shifts the level of the signal output from the waveform processing circuit, and the waveform processing circuit being connected to a negative reference voltage input terminal, to which the negative voltage is input, and a negative supply voltage input terminal, to which a negative supply voltage having a predetermined voltage referred to the negative reference voltage (VSS in figure 3).

With respect to claim 8, Choi teaches a power supply terminal for supplying a drive power supply of the input amplifier circuits of the plurality of drive systems, and a power supply terminal for supplying a drive power supply of the output amplifier circuits of the plurality of drive systems and the negative supply voltage input terminal, are separately provided (VDD, VB, and VCC in figure 3).

With respect to claim 9, Choi teaches the waveform processing circuit being a Schmitt trigger circuit (column 4, lines 15-25).

With respect to claim 10, Choi teaches the waveform processing circuit being a Schmitt trigger circuit (column 4, lines 15-25).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 15-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,502,412 to Choi et al. in view of U.S. Patent Application Publication No. 2002/0175883 to Onozawa et al.

Claims 15, 17, and 19 require the pre-drive circuit include two of the drive systems. Although not explicitly stated, it would have been obvious to one having ordinary skill in the art to utilize two of the drive systems in the pre-drive circuit. The motivation for doing so would have been to drive a plurality of loads.

Claims 16 and 18 require the pre-drive circuit include four of the drive systems. Although not explicitly stated, it would have been obvious to one having ordinary skill in the art to utilize four of the drive systems in the pre-drive circuit. The motivation for doing so would have been to drive a plurality of loads.

With respect to claims 20 and 26-31, Choi teaches the pre-drive circuit set forth in claim 15. Claim 20 requires a first switch element be connected to an output of the output amplifier circuit of one of the plurality of drive system of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a

capacitive load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element. Onozawa teaches such a configuration (SW15 being the first switch; D5 and Q28 and Q29 being the second switch; figure 6). At the time of the invention, it would have been obvious to one having ordinary skill in the art to utilize the switching and capacitive load system of Onozawa in the driving system of Choi. The motivation for doing so would have been to provide desired switching capabilities, such as high-speed switching, or switching between a plurality of capacitive loads.

With respect to claim 21, Choi teaches the pre-drive circuit set forth in claim 15. Claim 21 requires a first switch element be connected to an output of the output amplifier circuit of one of the plurality of drive system of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a capacitive load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element. Onozawa teaches such a configuration (SW15 being the first switch; D5 and Q28 and Q29 being the second switch; figure 6). Claim 21 further requires a second pre-drive circuit as set forth in claim 15, and third and fourth switches associated with the second pre-drive circuit, in a similar manner to the first and second switches being associated with the first pre-drive circuit as outlined above, wherein the high level voltage be supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage be supplied to the capacitive load via the fourth switch and a second coil

connected in series to the fourth switch element. Onozawa teaches such a configuration (Q33 and Q34 and associated coils in figure 6). At the time of the invention, it would have been obvious to one having ordinary skill in the art to utilize the switching setup of Onozawa in the system as taught or suggested by Choi. The motivation for doing so would have been to provide desired switching capabilities, such as high-speed switching, or switching between a plurality of capacitive loads.

With respect to claim 22, Choi teaches the pre-drive circuit set forth in claim 16. Claim 22 requires a first switch element be connected to an output of the output amplifier circuit of one of the plurality of drive system of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a capacitive load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element. Onozawa teaches such a configuration (SW15 being the first switch; D5 and Q28 and Q29 being the second switch; figure 6). Claim 22 further requires a second pre-drive circuit as set forth in claim 16, and third and fourth switches associated with the second pre-drive circuit, in a similar manner to the first and second switches being associated with the first pre-drive circuit as outlined above, wherein the high level voltage be supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage be supplied to the capacitive load via the fourth switch and a second coil connected in series to the fourth switch element. Onozawa teaches such a configuration (Q33 and Q34 and associated coils in figure 6). At the time of the

invention, it would have been obvious to one having ordinary skill in the art to utilize the switching setup of Onozawa in the system as taught or suggested by Choi. The motivation for doing so would have been to provide desired switching capabilities, such as high-speed switching, or switching between a plurality of capacitive loads.

With respect to claims 23, 32, and 33, Choi teaches the pre-drive circuit set forth in claim 17. Claim 23 requires a first switch element be connected to an output of the output amplifier circuit of one of the plurality of drive systems of the drive systems of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a capacitive load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element. Onozawa teaches such a configuration (SW15 being the first switch; D5 and Q28 and Q29 being the second switch; figure 6). At the time of the invention, it would have been obvious to one having ordinary skill in the art to utilize the switching and capacitive load systems of Onozawa in the driving system of Choi. The motivation for doing so would have been to provide desired switching capabilities, such as high-speed switching, or switching between a plurality of capacitive loads.

With respect to claim 24, Choi teaches the pre-drive circuit set forth in claim 17. Claim 24 requires a first switch element be connected to an output of the output amplifier circuit of one of the plurality of drive system of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a capacitive

load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element. Onozawa teaches such a configuration (SW15 being the first switch; D5 and Q28 and Q29 being the second switch; figure 6). Claim 24 further requires a second pre-drive circuit as set forth in claim 17, and third and fourth switches associated with the second pre-drive circuit, in a similar manner to the first and second switches being associated with the first pre-drive circuit as outlined above, wherein the high level voltage be supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage be supplied to the capacitive load via the fourth switch and a second coil connected in series to the fourth switch element. Onozawa teaches such a configuration (Q33 and Q34 and associated coils in figure 6). At the time of the invention, it would have been obvious to one having ordinary skill in the art to utilize the switching setup of Onozawa in the system as taught or suggested by Choi. The motivation for doing so would have been to provide desired switching capabilities, such as high-speed switching, or switching between a plurality of capacitive loads.

With respect to claim 25, Choi teaches the pre-drive circuit set forth in claim 18. Claim 25 requires a first switch element be connected to an output of the output amplifier circuit of one of the plurality of drive system of the pre-drive circuit; and a second switch element connected to an output of the output amplifier circuit of the other of the plurality of drive systems, wherein a high level voltage is supplied to a capacitive load via the first switch element and a low level voltage is supplied to the capacitive load via the second switch element. Onozawa teaches such a configuration (SW15 being

the first switch; D5 and Q28 and Q29 being the second switch; figure 6). Claim 25 further requires a second pre-drive circuit as set forth in claim 18, and third and fourth switches associated with the second pre-drive circuit, in a similar manner to the first and second switches being associated with the first pre-drive circuit as outlined above, wherein the high level voltage be supplied to the capacitive load via the third switch element and a first coil connected in series to the third switch element, and the low level voltage be supplied to the capacitive load via the fourth switch and a second coil connected in series to the fourth switch element. Onozawa teaches such a configuration (Q33 and Q34 and associated coils in figure 6). At the time of the invention, it would have been obvious to one having ordinary skill in the art to utilize the switching setup of Onozawa in the system as taught or suggested by Choi. The motivation for doing so would have been to provide desired switching capabilities, such as high-speed switching, or switching between a plurality of capacitive loads.

With respect to claims 34 and 35, Onozawa teaches a plasma display apparatus comprising: a plurality of Y electrodes arranged adjacently to the plurality of X electrodes by turns and each causing a discharge to occur between the neighboring X and Y electrodes (figure 4); an X electrode drive circuit (3) for applying a discharge voltage to the plurality of X electrodes; and a Y electrode drive circuit (5) for applying a discharge voltage to the plurality of Y electrodes, wherein at least one of the X electrode drive circuit (figure 6) and the Y electrode drive circuit (figure 5) is the capacitive load drive circuit set forth in claim 20.

Citation of Pertinent References

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patent documents further show the state of the art with respect to driving circuits:

a. U.S. Patent No. 6,885,225 B2 to Ohmichi et al.

b. European Patent Application EP 1 139 323 A2

Communication Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leith A. Al-Nazer whose telephone number is 571-272-1938. The examiner can normally be reached on Monday-Friday, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LA

HOANG V. NGUYEN
PRIMARY EXAMINER